REMARKS/ARGUMENTS

Claims 1-19 are pending in the Application. By this Amendment, claims 1 and 10 are being amended to improve their form. No new matter is involved.

In Paragraph 2 which begins on page 2 of the Office Action, claims 1-4, 8-11 and 19 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,771,031 of Kinoshita et al. In Paragraph 4 which begins on page 4 of the Office Action, claims 5-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kinoshita et al. '031. In Paragraph 5 which begins on page 5 of the Office Action, claims 12-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kinoshita et al. '031 in view of U.S. Patent 6,020,871 of Asada. These rejections are respectfully traversed.

According to the Office Action, Kinoshita et al. teaches a display panel having a plurality of pixels arrayed in a matrix, the pixels in each row forming one horizontal pixel array, and a plurality of block driving circuits arranged in series to divide pixels in each horizontal pixel array to a plurality of pixel blocks, for driving the pixel blocks. Kinoshita et al. is said to teach that each of the driver sections XT1 to XT8 is constituted by a shift register circuit SR of 100 stages (or bits) (input-side line memory), a selection circuit SA, a latch circuit LA1, a latch circuit LA2 (output-side line memory), and a digital-analog converter D/A. Kinoshita et al. is also said to teach in the driver section XT1, that first to hundredth stages of the shift register store a start pulse ST in turns in response to clock pulses CK. The selection circuit SA selects a corresponding one of hundred RGB pixel data items sequentially supplied to data supply bus SDL1 as a RGB pixel-data block DB1, in response to a signal from a stage which stores the start pulse ST, and supplies three pixel data items of the selected RGB pixel data to the latch circuit LA1, simultaneously. The latch circuit LA1 is said to latch each of the pixel data items

sequentially supplied from the selection circuit SA in correspondence with hundred RGB pixel data items, and supplies the pixel data items into the latch circuit LA2. The latch circuit LA2 latches all of the pixel data items from the latch circuit LA1 in response to a load pulse LD, and supplies the pixel data items to the digital-analog converter D/A. The digital-analog converter D/A converts the pixel data items into pixel signal voltages, respectively, and supplies to signal lines X1 to X300.

However, a careful review of Kinoshita et al. shows that the present invention clearly differs from the device described in such reference. An important and distinctive feature of the present invention that the data which the memory stores and outputs is video data, is not disclosed by Kinoshita et al. Independent claims 1 and 10 are being amended in order to better emphasize this feature in accordance with the invention. As so amended, each claim recites "a plurality of memory portions storing the digital data which is digital video data assigned by said data separation portion" (emphasis added).

Further differences exist between the present invention and Kinoshita et al. According to the Office Action, the shift register SR of 100 stages (or bits) of Kinoshita et al. is said to correspond to the "input-side line memory" of the present invention. However, and as indicated in the Office Action itself, the first to hundredth stages of the shift register SR of Kinoshita et al. stores a "start pulse ST" in turns in response to clock pulses CK. Therefore, the shift register of Kinoshita et al., which is indicated in the Office Action as corresponding to the input-side line memory of the present invention, is instead a circuit for sequentially storing a start pulse ST and then transferring it to the following stage, and therefore is not a circuit for storing digital data which is "digital video data" assigned to the data separation portion as achieved by the input-side line memory of the present invention.

Further in Kinoshita et al., the selection circuit SA extracts data from the data supply bus SDL1 or SDL2 in accordance with the start pulse output from each of the first to hundredth stages of the shift register SR, and supplies the extracted data to the latch circuit LA1. In other words, the shift register SR outputs a signal for controlling the timing for extracting serial data by the selection circuit SA. Considering the typical function of the shift register, it is clear that the "start pulse ST" which is stored is not "transferred in parallel" to the selection circuit SA provided at the following stage.

Therefore, as described above, the shift register SR of Kinoshita et al. is clearly different from the "input-side line memory" of the present invention.

The Office Action also refers to the latch circuit LA2 of Kinoshita et al. as corresponding to the "output-side line memory" of the present invention. The latch circuit LA2 of Kinoshita et al. outputs, "in parallel", the data transferred from the latch circuit LA1 to the digital-analog converter D/A in response to a load signal LD.

On the contrary, the "output-side line memory" of the present invention holds the data transferred from the input-side line memory and has a plurality of output portions "capable of serially outputting the data held therein from prescribed positions different from each other", and therefore completely differs from the latch circuit LA2 of Kinoshita et al. In addition, Kinoshita has no description or suggestion concerning the feature of "serially outputting data from prescribed positions different from each other" as achieved by the "output-side line memory" of the present invention.

Moreover, although not pointed out in the Office Action, Kinoshita et al. discloses memories M1 to M3 for holding and outputting the display data in Figs. 4, 6 and 7, for example. However, as can be understood from the timing chart of Fig. 5, when attention is paid to each memory M1 to M3, the memory M1, M2, or

M3 merely stores the supplied serial data at the address designated by a writing address signal WADRS and sequentially outputs the data from the address designated by the reading address signal RADRS. In other words, Kinoshita describes the memories M1 to M3 each performing mere data input and output, and does not describe memories having functions such as the "input-side line memory" and the "output-side line memory" as provided by the present invention. Clearly, the memories M1 to M3 are not provided with the function of the input-side line memory for transferring the data held therein to the output-side line memory in parallel or with the function of the output-side line memory having a plurality of output portions capable of serially outputting the data transferred from the input-side line memory and held therein from prescribed positions different from each other.

Independent claims 1 and 10 emphasize such feature in accordance with the invention by reciting "output-side line memory for holding the serial data stored in said input-side line memory and transferred in parallel from said input-side line memory and having a plurality of output portions capable of serially outputting the data held therein from prescribed positions different from each other ".

As described above, neither the "input-side line memory" or the "output-side line memory" of the present invention is described in Kinoshita et al., and it is therefore not possible to anticipate or suggest the present invention in view of such reference.

Consequently, independent claims 1 and 10 are submitted to clearly distinguish patentably over Kinoshita et al. Claims 2-9 and 11-19 depend, directly or indirectly, from one of independent claims 1 and 10, and contain all of the limitations thereof, so that such claims are also submitted to clearly distinguish patentably over the reference.

In rejecting claims 12-18 as unpatentable over the attempted combination of Kinoshita et al. and Asada, Asada is said to teach a bi-directional scanning circuit applicable when a plurality of IC chips are connected in cascade. However, Asada fails to remedy the basic deficiencies of the principal reference of Kinoshita et al., so that claims 12-18 are submitted to clearly distinguish patentably over such attempted combination.

In conclusion, claims 1-19 are submitted to clearly distinguish patentably over the cited art for the reasons described above. Therefore, reconsideration and allowance are respectfully requested.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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By: _____
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701